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Attorney's Docket No. 2200-306 PATENT CC 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wen-Chih Chiou
Serial No.: 09/ 761,486
Filed: Jan. 16, 2001
For: Method for Adjusting Optical Properties of an Anti-Reflective Coating Layer

Group Art Unit: 1762
Examiner: Markham, Wesley D.

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on Sept. 3, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
___ small entity $165.00
X other than a small entity $330.00

Appeal Brief fee due: $ 330.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))
I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EL 995 797 587 US in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313

Dated: 11/3/03

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 420.00	$210.00
☐	three months	$ 950.00	$475.00
☐	four months	$1,480.00	$740.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 330.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 330.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 330.00
X Credit Card Payment Form in the sum of $ 330.00 .
A duplicate copy of this transmittal is attached.

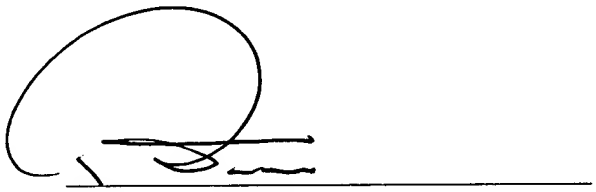
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor to charge Deposit Account No. 50-0484

And/Or

__X__ If any additional fee for claims is required, please charge Deposit Account No. 50-0484



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Wen-Chih Chiou

Group Art Unit: 1762

Serial No.: 09/761,486

Examiner: Markham, Wesley D.

Filed: Jan. 16, 2001

For: Method for Adjusting Optical Properties of an Anti-Reflective Coating Layer

Attorney Docket No.: 67,200-306

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EL 995 797 587 US
Date of Deposit Nov. 3, 2003

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $330.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal, Commissioner for Patents, Alexandria, VA 22313-1450.

Kathy Dixon

APPEAL BRIEF

Mail Stop: Appeal
Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Appellants appeal in the captioned application from the Examiner's final rejection, dated June 6, 2003, of claims 1-2, 5-7 and 9-17, under 35 USC §103(a) as being unpatentable over Plat et al '751, Holscher et al '292, Demirlioglu et al '704, Sandhu et al '282, Lee '672 and Yao '734.

It is urged that the rejection be reversed and that all the claims be allowed.

(1) **REAL PARTY IN INTEREST**

The real party in interest in the present appeal is the recorded Assignee of Taiwan Semiconductor Manufacturing Company, Ltd.

(2) **RELATED APPEALS AND INTERFERENCES**

There are no other appeals or interferences that are known to the Appellants, the Appellants' legal representative, or the assignee.

(3) **STATUS OF CLAIMS**

Claims 1-2, 5-7 and 9-17 are pending in the application.

Claims 1-2, 5-7 and 9-17 stand rejected.

No claims stand allowed.

(4) **STATUS OF AMENDMENTS**

A Request For Reconsideration was filed on or about August 6, 2003, which does not contain any claim amendments.

An Advisory Action was received from the Examiner dated September 24, 2003, maintaining rejection of all claims.

A Notice of Appeal was filed on or about September 3, 2003.

(5) SUMMARY OF THE INVENTION

The invention relates to a method for adjusting an extinction coefficient of a dielectric, anti-reflective coating layer by annealing at a temperature of at least 400°C in a gas environment that includes at least one of O_2 and N_2.

(Specification, page 1, lines 7-10)

In a preferred embodiment, the method for adjusting the optical properties of an anti-reflective coating layer can be carried out by first providing a preprocessed semiconductor substrate that has a silicon nitride or a polysilicon layer deposited on top, then depositing a dielectric ARC layer on the silicon nitride or polysilicon layer, then annealing the dielectric ARC layer deposited on the semiconductor substrate at a temperature of at least 400°C and in a gas environment including at least one of N_2 and O_2.

(Specification, page 7, lines 7-15)

In the method for adjusting the optical properties of a dielectric ARC layer, the dielectric anti-reflective coating layer is deposited of a material selected from the group consisting of SiO_2, SiON and SiONH. The method may further include the step of annealing the dielectric ARC layer at a temperature between about 400°C and about 1,000°C. The method may further include the step

of annealing the dielectric ARC layer for a timer period between about 1 min. and about 30 min., preferably between about 3 min. and about 5 min. The method may further include the step of adjusting the optical properties of the dielectric ARC layer to a reflective index (n) between about 2.0 and about 2.5, and an extinction coefficient (k) between about 0.2 and about 0.8.

(Specification, page 8, lines 7-18)

(6) ISSUES

Issue I

Is the rejection of claims 1-2, 5, 9-11 and 13-17 under 35 USC §103(a) as being unpatentable over Plat et al '751 in view of Holscher et al '292 proper when such references do not teach or suggest the specifically claimed limitations in the present application?

Issue II

Is the rejection of claims 6 and 7 under 35 USC §103(a) as being unpatentable over Plat et al in view of Holscher et al and further in view of Demirlioglu et al '704 proper when such references do not teach or suggest the specifically claimed limitations in the present application?

Issue III

Is the rejection of claims 1-2, 6, 9-11 and 13-16 under 35 USC §103(a) as being unpatentable over Holscher et al and Plat et al proper when such references do not teach or suggest the specifically claimed limitations in the present application?

Issue IV

Is the rejection of claims 5, 7 and 17 under 35 USC §103(a) as being unpatentable over Holscher et al , Plat et al and further in view of Sandhu et al '282 proper when such references do not teach or suggest the specifically claimed limitations in the present application?

Issue V

Is the rejection of claim 12 under 35 USC §103(a) as being unpatentable over Holscher et al, Plat et al and further in view of Lee '672 and Yao '734 proper when such references do not teach or suggest the specifically claimed limitations in the present application?

(7) GROUPING OF CLAIMS

The rejection of claims 1-2, 5, 9-11 and 13-17 are contested as a group.

The rejection of claims 6 and 7 are contested as a separate group.

The rejection of claims 1-2, 6, 9-11 and 13-16 are contested as a separate group.

The rejection of claims 5, 7 and 17 are contested as another separate group.

The rejection of claim 12 is contested as a further separate group.

The claims stand or fall together within their respective groups.

(8) **ARGUMENTS**

Issue I

Claims 1-2, 5, 9-11 and 13-17 are rejected under 35 USC §103(a) as being unpatentable over Plat et al '751 in view of Holscher et al '292.

In the Response to Arguments section of the 06/06/2003 Office Action, the Examiner argued that, "the condensing step of Plat et al decreases the thickness of the ARC layer, a process that would necessarily affect and alter the anti-reflective properties of an ARC". Furthermore, while the Examiner agrees with the Appellants that the stated purpose of the annealing process of Plat et al is different from the stated purpose of the Appellants'

claimed process, the Examiner nevertheless concluded that, "the combination of Plat et al and Holscher et al teaches all the process steps and limitations of the Appellants' claims, including the type of substrate, the nature of the ARC, the annealing temperature, the annealing time, and the type of gas used in the annealing process". The Examiner further concluded that, "therefore, the method of the combination of Plat et al and Holscher et al would have inherently adjusted the optical properties, such as the extinction coefficient, of the ARC layer as claimed by the Appellants".

The rejection of claims 1-2, 5, 9-11 and 13-17 under 35 USC §103(a) based on Plat et al '751 and Holscher et al is improper and must be reversed.

Plat et al discloses a method for reducing ARC layer removal by condensing the ARC layer. As stated by Plat et al at col. 5, lines 60+:

> "The ARC layer is then condensed to approximately the desired thickness, via step 106. The condensing step 106 preferably condenses the ARC layer by about 30%. In the condensing step, the ARC layer therefore increases in density and decreases in thickness ... because the ARC layer has been condensed, the ARC layer is less

> subject to removal during a first resist strip and clean ... Furthermore, **condensing the ARC layer does not adversely affect the anti-reflective properties of the ARC layer.**"

The Plat et al's process achieves a completely different result than that achieved by the present invention, and therefore, is used for a completely different purpose than the method of the present invention. In the present invention method, the specific combination of the dielectric ARC layer/substrate surface is used to maximize the compatibility between the two. The Plat et al's reference is not concerned with the compatibility problem between an ARC layer and its substrate, i.e. the Plat et al reference does not recognize such a compatibility problem. As such, the Plat et al's method does not provide a solution to solve such problem. In other words, **Plat et al does not teach the desirability or the need to use other than SiON ARC material.**

The present invention, to the contrary, clearly shows the desirability and the necessity of utilizing an SiONH or SiO_2 dielectric ARC layer on a substrate surface of polysilicon or silicon nitride. For instance, independent claim 1 clearly recites:

> "depositing a dielectric ARC layer on said SiN_x or said polysilicon layer wherein said dielectric ARC layer is deposited of a material selected from the group consisting of SiO_2 and SiONH."

Furthermore, in the present invention specification page 3, line 8 through page 4, line 1:

> "The **surface of a polysilicon layer or a silicon nitride layer is also highly reflective**, almost matching that of an aluminum layer. The high reflectivity of the surface of polysilicon or silicon nitride renders an imaging process for lithography difficult to carry out. The use of an anti-reflective coating layer on top of the polysilicon or the silicon nitride prior to depositing a photoresist layer is therefore necessary. **For compatibility reasons, a dielectric type anti-reflective coating material is more suitable for coating the polysilicon or the silicon nitride surface.**"

The present invention is therefore aimed to solve a specific problem, that was not even recognized by either Plat et al nor Holscher et al, of compatibility between layers of different materials. It is only the present invention that recognizes such problem, and therefore, it is only the present invention that teaches a solution to such problem, i.e. **a specific structure of**

dielectric ARC materials of SiONH or SiO_2 on top of polysilicon or SiN_x surfaces. This is neither taught or disclosed by Plat et al or Holscher et al, either singularly or in combination thereof.

A rejection under 35 USC §103 must rest on a factual basis. In re Warner, 379 F2d 1011, 154 USPQ 173 (CCPA 1967). "The Examiner, who has the duty of advancing this factual basis, may not, because he or she doubts that the claimed invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in the factual basis." Id.

In the present case, the Appellants respectfully submit that the Examiner has made unfounded assumptions that condensing step of Plat et al does not necessarily affects the anti-reflective properties and ARC when there is no solid evidence to support such assumption in either Plat et al or Holscher et al. The conclusion drawn by the Examiner that the method of the combination of Plat et al and Holscher et al would have inherently adjusted the optical properties, of the ARC layer is mere speculation or hindsight reconstruction in an effort to supply deficiencies in the factual basis in view of Plat et al and Holscher et al.

The Appellants further submit that while the Examiner attempted to combine the Plat et al reference with the Holscher et al reference, the Appellants submit that **there can be no motivation for such combination.** The Appellants cannot find any suggestion in either reference as to the desirability of such modification. In re Brouwer, 37 USPQ 2d 1663(Fed. Cir. 1996). Without such suggestions made in either of the references, the basis for the selection of the references and the purported modification must undoubtedly be hindsight drawn from Appellants' disclosure. In re Oetiker, 24 USPQ 2d 1443 (Fed. Cir. 1992). In the present case, Plat et al does not contain any teaching or suggestion that their SiON ARC layer is not compatible with the substrate surface that SiON is coated on. Similarly, Holscher et al does not contain any teaching or suggestion that the SiONH ARC layer is especially compatible with certain substrate surfaces. Lacking such suggestion or desirability, there can be no motivation in combining the two references in arriving at the present invention method.

The rejection of claims 1-2, 5, 9-11 and 13-17 under 35 USC §103(a) based on Plat et al and Holscher et al is improper and must be reversed.

Issue II

Claims 6 and 7 are rejected under 35 USC §103(a) as being unpatentable over Plat et al in view of Holscher et al and further in view of Demirlioglu et al '704.

It is contended that while the combination of Plat et al and Holscher et al does not teach a method in which the gas used in annealing is N_2, however, such is taught by Demirlioglu et al.

Claims 6 and 7 depend on independent claim 1, which clearly recites a dielectric ARC layer of SiO_2 or SiONH on a substrate surface of SiN_x or polysilicon. The Appellants have clearly shown above that such is not taught or disclosed by either one or the combination of the two primary reference of Plat et al and Holscher et al. The Appellants therefore respectfully submit that the additional reference of Demirlioglu does not lend any additional weight in a §103(a) rejection of claims 6 and 7.

Issue III

Claims 1-2, 6, 9-11 and 13-16 are rejected under 35 USC §103(a) as being unpatentable over Holscher et al in view of Plat et al.

The rejection of claims 1-2, 6, 9-11 and 13-16 under 35 USC §103(a) based on Holscher et al and Plat et al is improper and must be reversed.

As previously presented, the Appellants have clearly shown that the combined teachings of Holscher et al and Plat et al does not teach the invention contained in independent claims 1 and 13 since neither reference recognizes the problem of compatibility, and therefore, neither reference provides such a solution, as provided by the present invention. Furthermore, neither reference contains any teachings on the desirability of such combination, i.e. Holscher et al does not teach that their SiONH ARC layer is especially suitable for improving compatibility with certain substrate surfaces, while Plat et al does not contain any teaching that SiON ARC layer is inadequate in any way due to compatibility problems.

The rejection of claims 1-2, 6, 9-11 and 13-16 under 35 USC §103(a) based on Holscher et al and Plat et al is improper and must be reversed.

Issue IV

Claims 5, 7 and 17 are rejected under 35 USC §103(a) as being unpatentable over Holscher et al in view of Plat et al and further in view of Sandhu et al '282.

Dependent claims 5 and 7 depend on independent claim 1, while claim 17 depends on independent claim 13. As presented above, the Appellants have clearly shown that independent claims 1 and 13 are not rendered obvious based on Holscher and Plat since neither reference recognizes the desirability of improving compatibility between different material layers, and therefore, neither reference has provided such solution. The Appellants respectfully submit the additional reference of Sandhu et al, while teaching an annealing environment of O_2, does not lender any additional weight in a §103(a) rejection. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Issue V

Claim 12 is rejected under 35 USC §103(a) as being unpatentable over Holscher et al in view of Plat et al and further in view of either Lee '672 or Yao '734.

Dependent claim 12 depends on independent claim 1, which the Appellants have clearly shown is not rendered obvious based on the Holscher and Plat references. While the Appellants do not dispute that Lee or Yao et al teaches specific ranges of refractive indexes and range of extinction coefficients of certain typical ARC layers, the Appellants respectfully submit that the basic process defined by claim 1 of utilizing a specific combination of SiO_2 or SiONH ARC layers on top of a specific substrate surface of SiN_x or polysilicon is not taught or disclosed by either one of the two primary references. The additional references of Lee and Yao do not lend any additional weight in a §103 rejection of claim 12.

CLOSING

In summary, the Appellants have shown that their claimed invention is fully supported by a body of evidence of non-obviousness. It is respectfully submitted that such evidence of non-obviousness overcomes any showing of obviousness presented by the Examiner. The Appellants therefore submit that the final rejection of their claims 1-2, 5-7 and 9-17 is improper under 35 USC §103(a). The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

By: _____

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RWT\kd

CLAIM APPENDIX

1. (Previously Amended) A method for adjusting the optical properties of an anti-reflective coating (ARC) layer comprising the steps of:

providing a preprocessed semiconductor substrate having a SiN_x or a polysilicon layer on a top surface;

depositing a dielectric ARC layer on said SiN_x or said polysilicon layer wherein said dielectric ARC layer is deposited of a material selected from the group consisting of SiO_2 and SiONH; and

annealing said dielectric ARC layer deposited on said semiconductor substrate at a temperature of at least 400°C.

2. (Previously Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1 wherein said dielectric ARC layer deposited is SiONH.

3. - 4. (Cancelled)

5. (Previously Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1, wherein a gas used in said annealing process is O_2.

6. (Previously Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1, wherein a gas used in said annealing process is N_2.

7. (Previously Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1, wherein a gas used in said annealing process is a mixture of O_2 and N_2.

8. (Cancelled)

9. (Original) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1 further comprising the step of annealing said dielectric anti-reflective coating layer at a temperature between about 400°C and about 1,000°C.

10. (Original) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1 further comprising the step of annealing said dielectric anti-reflective coating layer for a time period between about 1 min. and about 30 min.

11. (Previously Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1 further comprising the step of annealing said dielectric anti-reflective coating layer for a time period between about 3 min. and about 5 min.

12. (Previously Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1 further comprising the step of adjusting said optical properties of the dielectric anti-reflective coating layer to a refractive index (n) between about 2.0 and about 2.5, and an extinction coefficient (k) between about 0.2 and about 0.8.

13. (Previously Amended) A method for adjusting the extinction coefficient (k) of a dielectric anti-reflective coating layer by the steps of:

providing a SiN_x or polysilicon layer covered semiconductor substrate;

depositing a dielectric anti-reflective coating layer of a material selected from the group consisting of SiO_2 and SiONH on top of said SiN_x or said polysilicon layer; and

heating said semiconductor substrate to a temperature between about 400°C and about 1,000°C in an environment that comprises at least one of N_2 or O_2.

14. (Previously Amended) A method for adjusting the extinction coefficient (k) of a dielectric anti-reflective coating layer according to claim 13 further comprising the step of heating said semiconductor substrate for a length of time sufficient to vary the extinction coefficient of said dielectric anti-reflective coating layer by at least 10%.

15. (Original) A method for adjusting the extinction coefficient (k) of a dielectric anti-reflective coating layer according to claim 13 further comprising the step of heating said semiconductor substrate for a length of time between about 1 min. and about 30 min.

16. (Original) A method for adjusting the extinction coefficient (k) of a dielectric anti-reflective coating layer according to claim 13 further comprising the step of heating said semiconductor substrate for a length of time between about 3 min. and about 5 min.

17. (Previously Amended) A method for adjusting the extinction coefficient (k) of a dielectric anti-reflective coating layer according to claim 13 further comprising the step of heating said semiconductor substrate to a temperature between 400°C and 700°C in an environment of O_2.